

CLAIMS

WHAT IS CLAIMED IS:

1. A method for providing a floating point product, comprising:
multiplying a subprecise operand and a non-subprecise operand using a plurality of intermediate stages; and
correcting an error introduced by the subprecise operand by performing an operation in conjunction with a one of the plurality of intermediate stages utilizing a compensating summand.
2. The method of claim 1, wherein multiplying the subprecise operand and the non-subprecise operand comprises using a multiplier array.
3. The method of claim 1, wherein correcting the error introduced by the subprecise operand further comprises:
determining the position of a delimiter bit contained within a first significand corresponding to the subprecise operand; and
generating the compensating summand utilizing the determined position of the delimiter bit, wherein the compensating summand is initially equal to a second significand corresponding to the non-subprecise operand.
4. The method of claim 3, wherein generating the compensating summand further comprises:

shifting the compensating summand so that the rightmost bit is aligned with the determined delimiter bit position;

logically inverting the compensating summand; and
adding a logical 1.

5. The method of claim 1, wherein the subprecise operand is represented using a delimited normalized format with an implicit leading 1-bit.

6. The method of claim 1, wherein the one of the plurality of intermediate stages is selected wherein a substantial time delay to correct the error is avoided.

7. The method of claim 1, wherein time consumed by multiplying the subprecise operand and the non-subprecise operand overlaps time consumed in correcting the error.

8. A system for providing a floating point product comprising a multiplying circuit for multiplying a subprecise operand and a non-subprecise operand using a plurality of intermediate stages, wherein an error introduced by the subprecise operand is corrected by performing an operation in conjunction with a one of the plurality of intermediate stages utilizing a compensating summand.

9. The system of claim 8, wherein the multiplying circuit comprises a multiplier array.

10. The system of claim 9, wherein the multiplier array uses 3-to-2 adders.

11. The system of claim 8, further comprising a creating circuit for creating the compensating summand comprising:

a determining circuit for determining the position of a delimiter bit contained within a first significand corresponding to the subprecise operand; and

a generating circuit for generating the compensating summand utilizing the determined position of the delimiter bit, wherein the compensating summand is initially equal to a second significand corresponding to the non-subprecise operand.

12. The system of claim 11, wherein the generating circuit further comprises:

a shifting circuit for shifting the compensating summand so that the rightmost bit is aligned with the determined delimiter bit position;

a logical inversion circuit for logically inverting the compensating summand; and

a producing circuit for producing a logical 1 to the compensating summand.

13. The system of claim 8, wherein the subprecise operand is represented using a delimited normalized format with an implicit leading 1-bit.

14. The system of claim 8, wherein the one of the plurality of intermediate stages is selected wherein a substantial time delay to correct the error is avoided.

15. The system of claim 8, wherein time consumed by multiplying the subprecise operand and the non-subprecise operand overlaps time consumed in correcting the error.

16. A computer-readable medium on which is stored a set of instructions for providing a floating point product, which when executed perform stages comprising:

 multiplying a subprecise operand and a non-subprecise operand using a plurality of intermediate stages; and

 correcting an error introduced by the subprecise operand by performing an operation in conjunction with a one of the plurality of intermediate stages utilizing a compensating summand.

17. The computer-readable medium of claim 16, wherein correcting the error introduced by the subprecise operand further comprises:

determining the position of a delimiter bit contained within a first
significand corresponding to the subprecise operand; and
calculating the compensating summand utilizing the determined position of
the delimiter bit, wherein the compensating summand is initially equal to a
second significand corresponding to the non-subprecise operand.

18. The computer-readable medium of claim 17, wherein generating
the compensating summand further comprises:

shifting the compensating summand so that the rightmost bit is aligned
with the determined delimiter bit position;

logically inverting the compensating summand; and

adding a logical 1.

19. The computer-readable medium of claim 16, wherein the
subprecise operand is represented using a delimited normalized format with an
implicit leading 1-bit.

20. The computer-readable medium of claim 16, wherein the one of the
plurality of intermediate stages is selected wherein a substantial time delay to
correct the error is avoided.

21. The computer-readable medium of claim 16, wherein time consumed by multiplying the subprecise operand and the non-subprecise operand overlaps time consumed in correcting the error.